Features

- **Three High-side and Three Low-side Drivers**
- **Outputs Freely Configurable as Switch, Half Bridge or H-bridge**
- **Capable of Switching All Kinds of Loads Such as DC Motors, Bulbs, Resistors, Capacitors and Inductors**
- **0.6 A Continuous Current Per Switch**
- **Low-side: R_{DSon} < 1.5 Ω Versus Total Temperature Range**
- **High-side: R_{DSon} < 2.0 Ω Versus Total Temperature Range**
- **Very Low Quiescent Current I_S < 20 µA in Standby Mode**
- **Outputs Short-circuit Protected**
- **Overtemperature Prewarning and Protection**
- **Undervoltage and Overvoltage Protection**
- **Various Diagnosis Functions Such as Shorted Output, Open Load, Overtemperature and Power Supply Fail**
- **Serial Data Interface**
- **Daisy Chaining Possible**
- **SSO20 Package**

Dual Triple DMOS Output Driver with Serial Input Control

T6817

Description

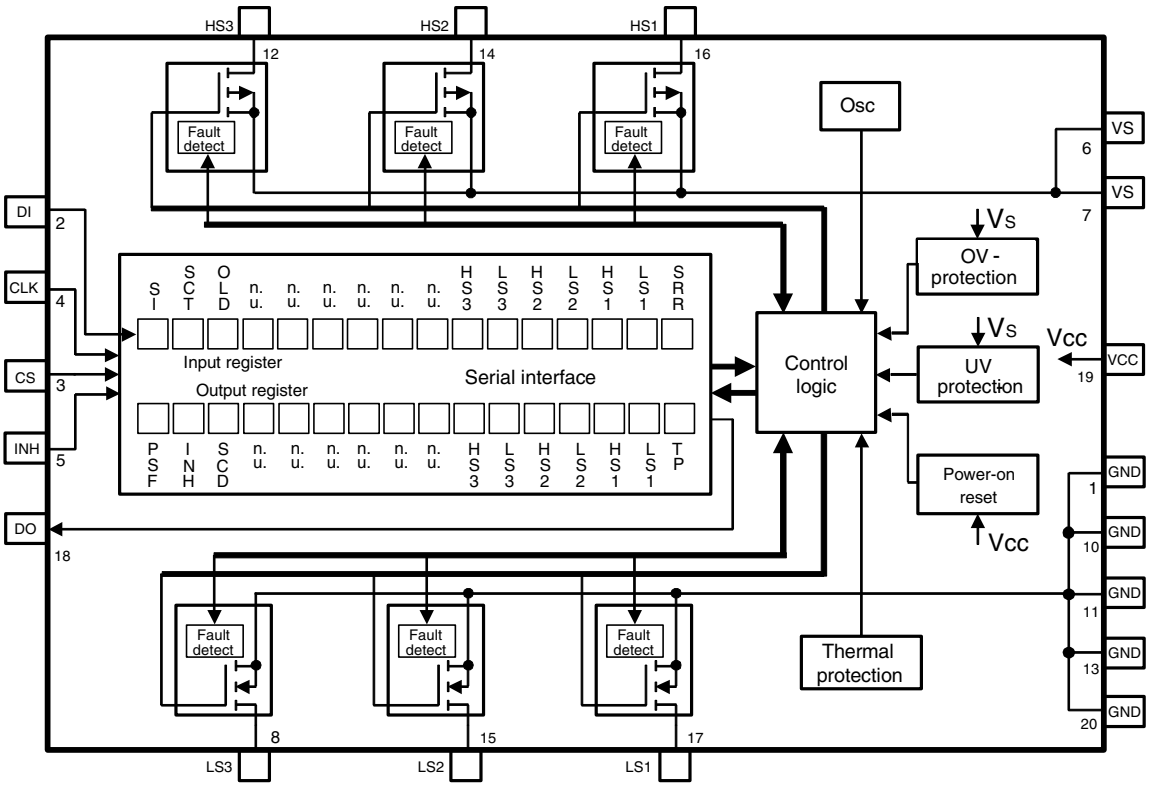
The T6817 is a fully protected driver interface designed in 0.8-µm BCDMOS technology. It can be used to control up to 6 different loads by a microcontroller in automotive and industrial applications.

Each of the 3 high-side and 3 low-side drivers is capable of driving currents up to 600 mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design is especially supportive of H-bridges applications to drive DC motors.

Protection is guaranteed in terms of short-circuit conditions, overtemperature, under- and overvoltage. Various diagnosis functions and a very low quiescent current in standby mode open a wide range of applications. Meeting automotive qualifications in the area of conducted interferences, EMC protection and 2 kV ESD protection provide added value and enhanced quality for the exacting requirements of automotive applications.

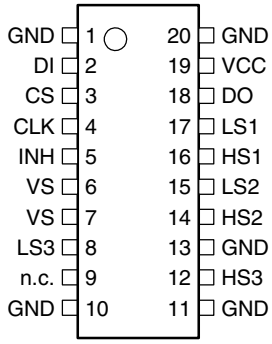
Rev. 4670A–BCD–02/03

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning SSO20



Pin Description

Pin	Symbol	Function
1	GND	Ground; reference potential; internal connection to Pin 10, 11, 13 and 20; cooling tab
2	DI	Serial data input; 5-V CMOS logic level input with internal pull-down; receives serial data from the control device, DI expects a 16-bit control word with LSB being transferred first
3	CS	Chip-select input; 5-V CMOS logic level input with internal pull-up; low = serial communication is enabled, high = disabled
4	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2 MHz)
5	INH	Inhibit input; 5-V logic input with internal pull-down; low = standby, high = normal operating
6, 7	VS	Power supply output stages HS1, HS2 and HS3
8	LS3	Low-side driver output 3; power-MOS open drain with internal reverse diode: overvoltage protection by active zenering; short-circuit protection; diagnosis for short and open load
9	n.c.	Not connected
10	GND	Ground (see Pin 1) be consistant
11	GND	Ground (see Pin 1)
12	HS3	High-side driver output 3; power-MOS open drain with internal reverse diode: overvoltage protection by active zenering; short-circuit protection; diagnosis for short and open load
13	GND	Ground (see Pin 1)
14	HS2	High-side driver output 2 (see Pin 12) be consistant
15	LS2	Low-side driver output 2 (see Pin 8)
16	HS1	High-side driver output 1 (see Pin 12)
17	LS1	Low-side driver output 1 (see Pin 8)
18	DO	Serial data output; 5-V CMOS logic level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first); output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on only one data output line only.
19	VCC	Logic supply voltage (5 V)
20	GND	Ground (see Pin 1)

Functional Description

Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, Pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3. Data Transfer Input Data Protocol

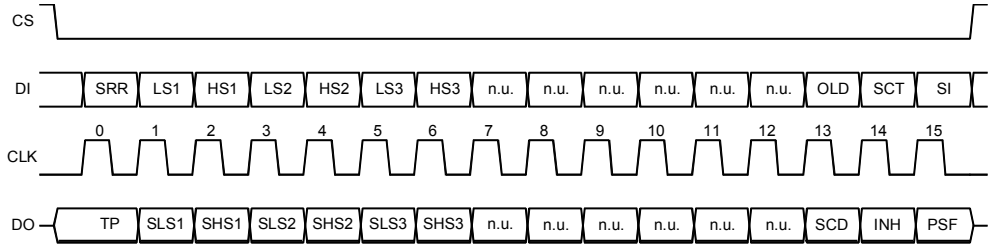


Table 1. Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n.u.	Not used
8	n.u.	Not used
9	n.u.	Not used
10	n.u.	Not used
11	n.u.	Not used
12	n.u.	Not used
13	OLD	Open load detection (low = on)
14	SCT	Programmable time delay for short circuit and overvoltage shutdown (short circuit shutdown delay high/low = 100 ms/12.5 ms, overvoltage shutdown delay high/low = 14 ms/3.5 ms
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered)

Table 2. Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning (overtemperature shutdown, see remark below)
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
3	Status LS2	Description, see LS1
4	Status HS2	Description, see HS1
5	Status LS3	Description, see LS1
6	Status HS3	Description, see HS1
7	n.u.	Not used
8	n.u.	Not used
9	n.u.	Not used
10	n.u.	Not used
11	n.u.	Not used
12	n.u.	Not used
13	SCD	Short circuit detected: set high, when at least one output is switched off by a short circuit condition
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (Pin 17). High = standby, low = normal operation
15	PSF	Power supply fail: over- or undervoltage at Pin VS detected

Note: Bit 0 to 15 = high: overtemperature shutdown

After power-on reset, the input register has the following status:

Bit 15 (SI)	Bit 14 (SCT)	Bit 13 (OLD)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	n.u.	n.u.	n.u.	n.u.	n.u.	n.u.	L	L	L	L	L	L	L

Power-supply Fail

In case of over- or undervoltage at Pin VS, an internal timer is started. When the undervoltage delay time (t_{dUV}, t_{dOV}) programmed by the SCT bit is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are enabled immediately. The PSF bit remains high until it is reset by the SRR bit in the input register.

Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{HS1-3}, I_{LS1-3}). If V_{VS}-V_{HS1-3} or V_{LS1-3} is lower than the open-load detection threshold (open-load condition), the corresponding bit of the output in the output register is set to high. Switching on an output stage with the OLD bit set to low disables the open-load function for this output. If bit SI is set to low, the open-load function is also switched off.

Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low, the state of TP appears at Pin DO. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the state of the input and output registers.

If the junction temperature exceeds the thermal shutdown threshold, $T_{j\ switch\ off}$, the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{j\ switch\ on}$, and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

Short-circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the overcurrent limitation and shutdown threshold (I_{HS1-3}, I_{LS1-3}) are reached. Simultaneously, an internal timer is started. The shorted output is disabled when during a permanent short the delay time (t_{dSd}) programmed by the short-circuit timer bit (SCT) is reached. Additionally, the short-circuit detection bit (SCD) is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled immediately and SCD bit is set. By writing a high to the SRR bit in the input register, the SCD bit is reset and the disabled outputs are enabled.

Inhibit

There are two ways to inhibit the T6817:

1. Set bit SI in the input register to zero
2. Switch Pin 5 (INH) to 0 V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 and by Pin 5 (INH) switched back to 5 V.

Absolute Maximum Ratings

All values refer to GND pins

Parameter	Pin	Symbol	Value	Unit
Supply voltage	6, 7	V_{VS}	- 0.3 to +40	V
Supply voltage t < 0.5 s; I_S > -2 A	6, 7	V_{VS}	- 1	V
Supply voltage difference $\lvert V_{S_Pin6} - V_{S_Pin7} \rvert$		ΔV_{VS}	150	mV
Supply current	6, 7	I_{VS}	1.4	A
Supply current t < 200 ms	6, 7	I_{VS}	2.6	A
Logic supply voltage	19	V_{VCC}	-0.3 to 7	V
Input voltage	5	V_{INH}	-0.3 to 17	V
Logic input voltage	2 to 4	$V_{DI,}$ $V_{CLK,}$ V_{CS}	-0.3 to V_{VCC} +0.3	V
Logic output voltage	18	V_{DO}	-0.3 to V_{VCC} +0.3	V
Input current	5, 2 to 4	$I_{INH,}$ $I_{DI,}$ $I_{CLK,}$ I_{CS}	-10 to +10	mA
Output current	18	I_{DO}	-10 to +10	mA
Output current	8, 12, 14 to 17	$I_{LS1\ to}$ I_{LS3} $I_{HS1\ to}$ I_{HS3}	Internal limited, see output specification	
Reverse conducting current (t_{Pulse} = 150 µs)	12, 14, 16 towards 6, 7	$I_{HS1\ to}$ I_{HS3}	17	A
Junction temperature range		T_j	-40 to +150	°C
Storage temperature range		T_{STG}	-55 to +150	°C

Thermal Resistance

All values refer to GND pins

Parameter	Test Conditions	Symbol	Value	Unit
Junction - pin	Measured to GND Pins 1, 10, 11, 13 and 20	R_{thJP}	25	K/W
Junction ambient		R_{thJA}	65	K/W

Operating Range

All values refer to GND pins

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins 6, 7	V_{VS}	V_{UV} (1)		40 (2)	V
Logic supply voltage	Pin 19	V_{VCC}	4.5	5	5.5	V
Logic input voltage	Pin 2 to 4 and 5	$V_{INH,}$ $V_{DI,}$ $V_{CLK,}$ V_{CS}	-0.3		V_{VCC}	V
Serial interface clock frequency	Pin 4	f_{CLK}			2	MHz
Junction temperature range		T_j	-40		150	°C

Notes: 1. Threshold for undervoltage detection
2. Outputs disabled for $V_{VS} > V_{OV}$ (threshold for overvoltage detection)

Noise and Surge Immunity

Parameter	Test Conditions	Value
Conducted interferences	ISO 7637–1	Level 4 [1)]
Interference Suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model)	MIL-STM 5.1 – 1998	2 kV
ESD (Machine Model)	JEDEC EIA / JESD 22 – A115-A	150 V

Note: 1. Test pulse 5: V_{Smax} = 40 V

Electrical Characteristics

7.5 V < V_{VS} < V_{OV}; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
1.1	Quiescent current (VS)	V_{VS} < 16 V, INH or bit SI = lo	6, 7	I_{VS}			40	µA	A
1.2	Quiescent current (VCC)	4.5 V < V_{VCC} < 5.5 V, INH or bit SI = low	19	I_{VCC}			20	µA	A
1.3	Supply current (VS)	V_{VS} < 16 V normal operating, all output stages off,	6, 7	I_{VS}		0.8	1.2	mA	A
1.4	Supply current (VS)	V_{VS} < 16 V normal operating, all output stages on, no load	6, 7	I_{VS}			10	mA	A
1.5	Supply current (VCC)	4.5 V < V_{VCC} < 5.5 V, normal operating Pin	19	I_{VCC}			150	µA	A
2	**Internal Oscillator Frequency**								
2.1	Frequency (time base for delay timers)			f_{OSC}	19		45	kHz	A
3	**Over- and Undervoltage Detection, Power-on Reset**								
3.1	Power-on reset threshold		19	V_{VCC}	3.4	3.9	4.4	V	A
3.2	Power-on reset delay time	After switching on V_{VCC}	19	t_{dPor}	30	95	160	µs	A
3.3	Undervoltage detection threshold		6, 7	V_{UV}	5.5		7.0	V	A
3.4	Undervoltage detection hysteresis		6, 7	ΔV_{UV}		0.4		V	A
3.6	Undervoltage detection delay		6, 7	t_{dUV}	7		21	ms	A
3.7	Overvoltage detection threshold		6, 7	V_{OV}	18.0		22.5	V	A
38	Overvoltage detection hysteresis		6, 7	ΔV_{OV}		1		V	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of CS after data transmission and switch on/off output stages to 90% of final level

Electrical Characteristics (Continued)

7.5 V < V_{VS} < V_{OV}; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.9	Undervoltage detection delay	Input register bit 14 (SCT) = high bit 14 (SCT) = low		 t_{dOV} t_{dOV}	 7 1.75		 21 5.25	 ms ms	A
4	**Thermal Prewarning and Shutdown**								
4.1	Thermal prewarning			T_{jPWset}	125	145	165	°C	A
4.2	Thermal prewarning			$T_{jPWreset}$	105	125	145	°C	A
4.3	Thermal prewarning hysteresis			ΔT_{jPW}	3	20		K	A
4.4	Thermal shutdown			$T_{j\ switch\ off}$	150	170	190	°C	A
4.5	Thermal shutdown			$T_{j\ switch\ on}$	130	150	170	°C	A
4.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$	3	20		K	A
4.7	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ off}$/ $T_{jPW\ set}$	1.05	1.17			A
4.8	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ on}$/ $T_{jPW\ reset}$	1.05	1.2			A
5	**Output Specification (LS1 - LS6, HS1 - HS6)** 7.5 V < V_{VS} < V_{OV}								
5.1	On resistance	I_{Out} = 600 mA	8, 15, 17	$R_{DS\ OnL}$			1.5	Ω	A
5.2	On resistance	I_{Out} = -600 mA	12, 14, 16	$R_{DS\ OnH}$			2.0	Ω	A
5.3	Output clamping voltage	I_{LS1-3}= 50 mA	8, 15, 17	V_{LS1-3}	40		60	V	A
5.4	Output leakage current	V_{LS1-3} = 40 V all output stages off	8, 15, 17	I_{LS1-3}			10	µA	A
5.5	Output leakage current	V_{HS1-3} = 0 V all output stages off	2, 3, 12, 13, 15, 28	I_{HS1-3}	-10			µA	A
5.7	Inductive shutdown energy		8, 12, 14 to 17	W_{outx}			15	mJ	D
5.8	Output voltage edge steepness		8, 12, 14 to 17	dV_{LS1-3}/dt dV_{HS1-3}/dt	50	200	400	mV/µs	A
5.9	Overcurrent limitation and shutdown threshold		8, 15, 17	I_{LS1-3}	650	950	1250	mA	A
5.10	Overcurrent limitation and shutdown threshold		12, 14, 16	I_{HS1-3}	-1250	-950	-650	mA	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of CS after data transmission and switch on/off output stages to 90% of final level

Electrical Characteristics (Continued)

7.5 V < V_{VS} < V_{OV}; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.11	Overcurrent shutdown delay time	Input register bit 14 (SCT) = high bit 14 (SCT) = low		 t_{dSd} t_{dSd}	 8 1.0	 12 1.5	 16 2.0	 ms ms	 A A
5.12	Open load detection current	Input register bit 13 (OLD) =low, output off	8, 15, 17	$I_{LS1–3}$	60		200	µA	A
5.13	Open load detection current	Input register bit 13 (OLD) =low, output off	12, 14, 16	$I_{HS1–3}$	-150		-30	µA	A
5.14	Open load detection current ratio			$I_{LS1–3}$ / $I_{HS1–3}$	1.2				A
5.15	Open load detection threshold	Input register bit 13 (OLD) =low, output off	8, 15, 17	$V_{LS1–3}$	0.6		4	V	A
5.16	Open load detection threshold	Input register bit 13 (OLD) =low, output off	12, 14, 16	$V_{VS–}$ $V_{HS1–3}$	0.6		4	V	A
5.17	Output switch on delay [1]	R_{Load} = 1 kΩ		t_{don}			0.5	ms	A
5.18	Output switch off delay [1]	R_{Load} = 1 kΩ		t_{doff}			1	ms	A
6	**Inhibit Input**								
6.1	Input voltage low level threshold		5	V_{IL}	0.3 × V_{VCC}			V	A
6.2	Input voltage high level threshold		5	V_{IH}			0.7 × V_{VCC}	V	A
6.3	Hysteresis of input voltage		5	ΔV_I	100		700	mV	A
6.4	Pull-down current	V_{INH} = V_{VCC}	5	I_{PD}	10		80	µA	A
7	**Serial Interface – Logic Inputs DI, CLK, CS**								
7.1	Input voltage low-level threshold		2-4	V_{IL}	0.3 × V_{VCC}			V	A
7.2	Input voltage high-level threshold		2-4	V_{IH}			0.7 × V_{VCC}	V	A
7.3	Hysteresis of input voltage		2-4	ΔV_I	50		500	mV	A
7.4	Pull-down current Pin DI, CLK	V_{DI}, V_{CLK} = V_{VCC}	2, 4	I_{PDSI}	2		50	µA	A
7.5	Pull-up current Pin CS	V_{CS}= 0 V	3	I_{PUSI}	-50		-2	µA	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of CS after data transmission and switch on/off output stages to 90% of final level

Electrical Characteristics (Continued)

7.5 V < V_{VS} < V_{OV}; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**Serial Interface - Logic Output DO**								
8.1	Output voltage low level	I_{OL} = 3 mA	18	V_{DOL}			0.5	V	A
8.2	Output voltage high level	I_{OL} = -2 mA	18	V_{DOH}	V_{VCC}- 1 V			V	A
8.3	Leakage current (tri-state)	$V_{CS} = V_{VCC}$, 0 V < V_{DO} < V_{VCC}	18	I_{DO}	-10		10	µA	A

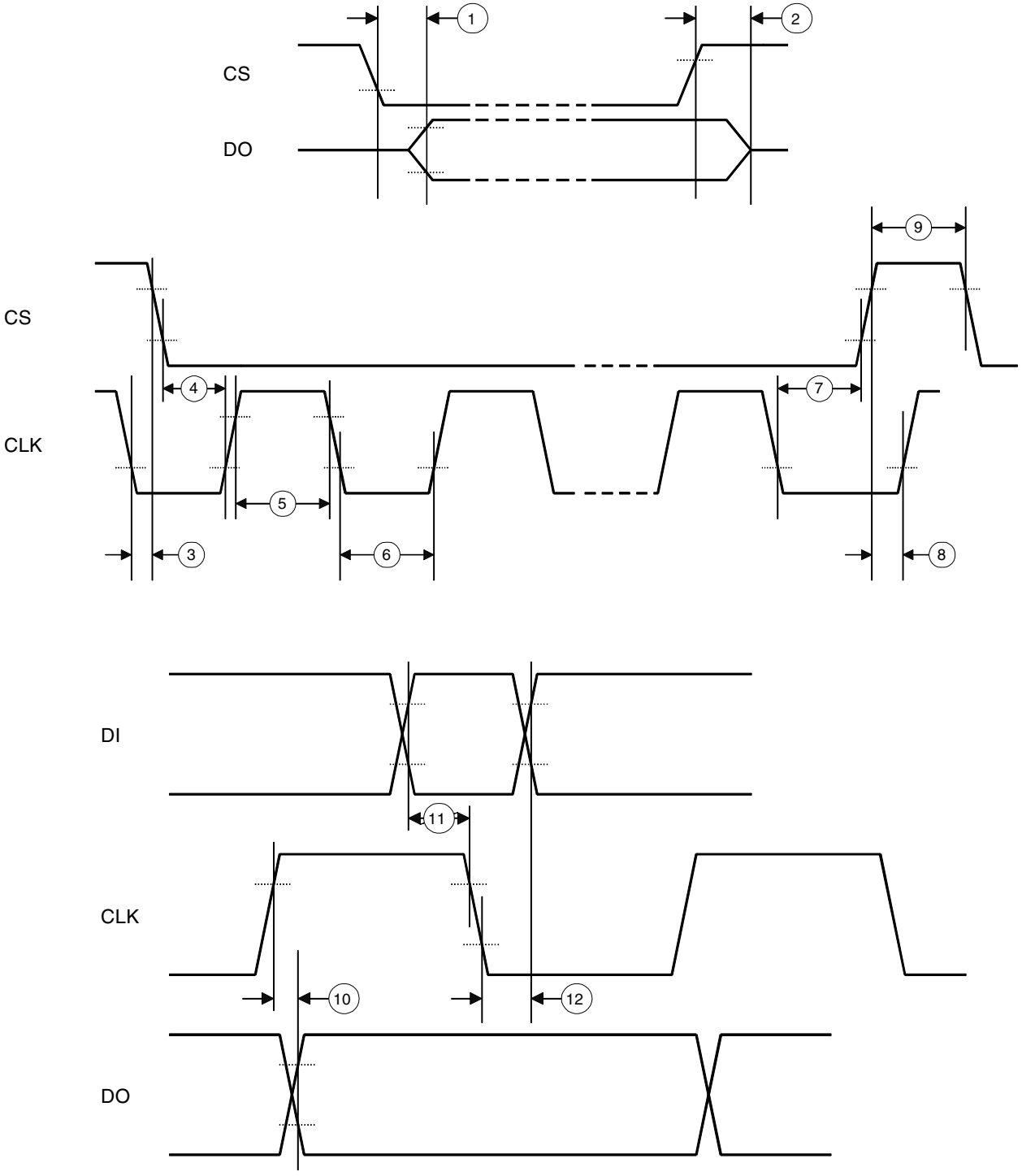
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of CS after data transmission and switch on/off output stages to 90% of final level

Serial Interface – Timing

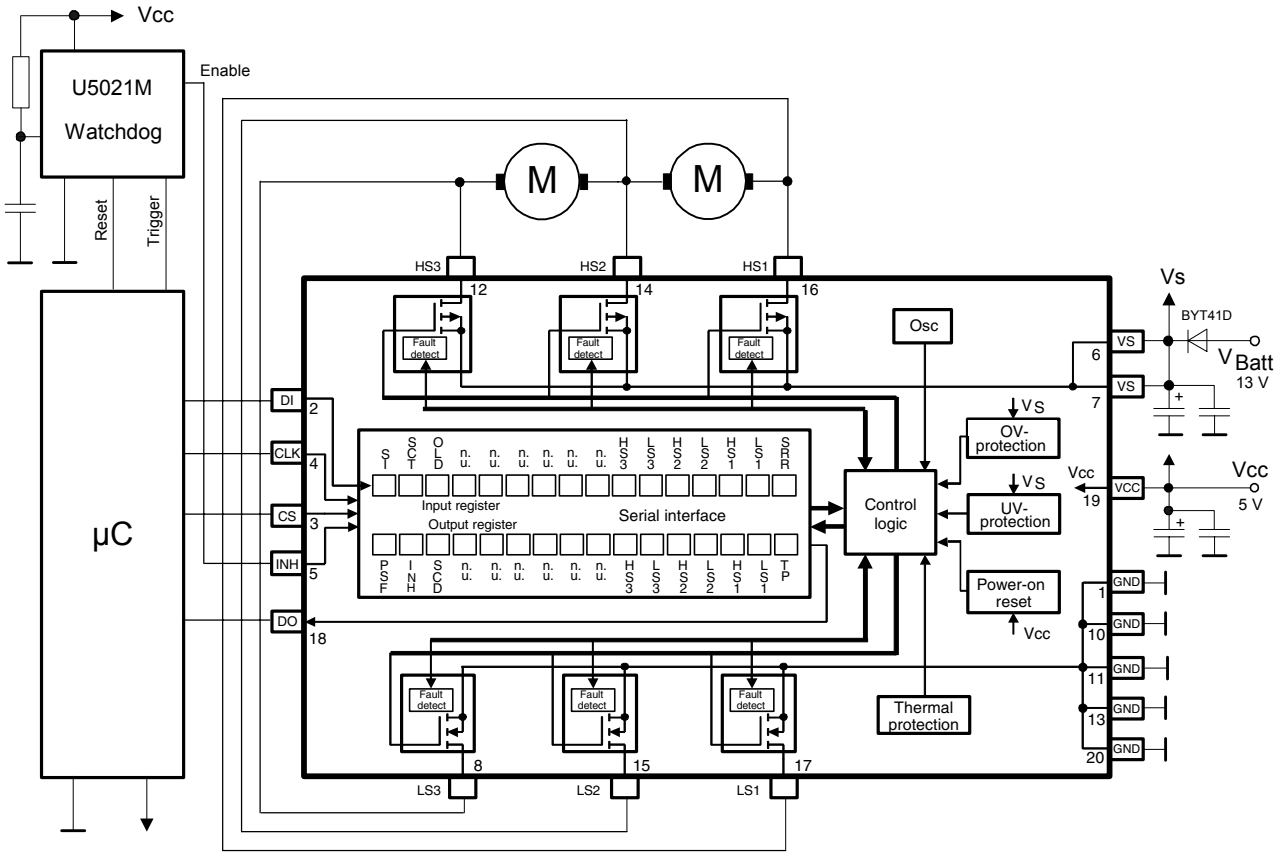
Parameters	Test Conditions	Timing Chart No.	Symbol	Min.	Typ.	Max.	Unit
DO enable after CS falling edge	C_{DO} = 100 pF	1	t_{ENDO}			200	ns
DO disable after CS rising edge	C_{DO} = 100 pF	2	t_{DISDO}			200	ns
DO fall time	C_{DO} = 100 pF	-	t_{DOf}			100	ns
DO rise time	C_{DO} = 100 pF	-	t_{DOr}			100	ns
DO valid time	C_{DO} = 100 pF	10	t_{DOVal}			200	ns
CS setup time		4	$t_{CSSethl}$	225			ns
CS setup time		8	$t_{CSSetlh}$	225			ns
CS high time	Input register Bit 14 (SCT) = high	9	t_{CSh}	140			ms
CS high time	Input register Bit 14 (SCT) = low	9	t_{CSh}	17.5			ms
CLK high time		5	t_{CLKh}	225			ns
CLK low time		6	t_{CLKl}	225			ns
CLK period time		-	t_{CLKp}	500			ns
CLK setup time		7	$t_{CLKSethl}$	225			ns
CLK setup time		3	$t_{CLKSetlh}$	225			ns
DI setup time		11	t_{DIset}	40			ns
DI hold time		12	t_{DIHold}	40			ns

Figure 4. Serial Interface Timing with Chart Numbers



Inputs DI, CLK, CS: High level = 0.7 x $V_{CC,}$ low level = 0.3 x V_{CC}
Output DO: High level = 0.8 x V_{CC}, low level = 0.2 x V_{CC}

Figure 5. Application Circuit



Application Notes

It is strongly recommended that the blocking capacitors at V_{CC} and V_S be connected as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:
Electrolythic capacitor C > 22 µF in parallel with a ceramic capacitor C = 100 nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{HSX} (see: Absolut Maximum Ratings).

Recommended value for capacitors at V_{CC}:
Electrolythic capacitor C > 10 µF in parallel with a ceramic capacitor C = 100 nF.

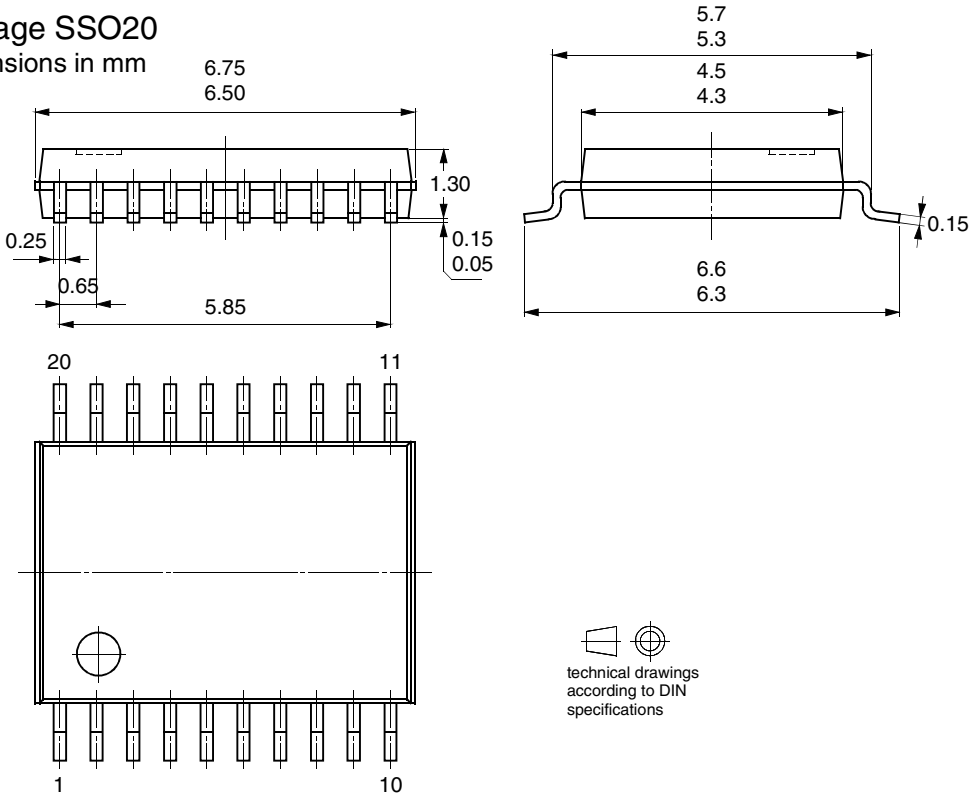
To reduce thermal resistance it is recommended that cooling areas be placed on the PCB as close as possible to GND pins.

Ordering Information

Extended Type Number	Package	Remarks
T6817-TKS	SSO20	Power package, tube
T6817-TKQ	SSO20	Power package, taped and reeled

Package Information

Package SSO20
Dimensions in mm



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